Ultra-Low dc Power GaAs HBT S- and C-Band Low Noise Amplifiers for Portable Wireless Applications

Kevin W. Kobayashi, *Member, IEEE*, Aaron K. Oki, *Member, IEEE*,
Liem T. Tran, *Member, IEEE*, and Dwight C. Streit, *Senior Member, IEEE*

***Abstract*— We report on a 2.1 mW low dc power GaAs HBT LNA with 2.0 dB noise figure and 8.9 dB gain at 2 GHz. This amplifier achieves a Gain/NF · P_{dc} ratio figure of merit of 2.10 (1/mW) which is the highest reported at S-band. Under low dc power bias of 2 V and 0.46 mA (0.92 mW), the amplifier achieves 5.2 dB gain, 3.01 dB noise figure and a Gain/P_{dc} figure of merit of 5.65 (dB/mW) which is also the highest reported in this frequency band. In addition, a 2-stage self-biased C-band LNA which achieves a minimum noise figure of 2.4 dB at 5 GHz, 16.2 dB gain, with only 72 mW of dc power was also demonstrated. This is believed to be the lowest noise figure performance so far reported for an HBT amplifier above 3 GHz. Both HBT LNA's are fabricated using a relaxed 3 μm emitter width low cost GaAs production foundry process. The high performance obtained from HBT's at very low dc bias makes them attractive for portable wireless applications in the Industrial-Scientific-Medical (ISM) frequency bands.**

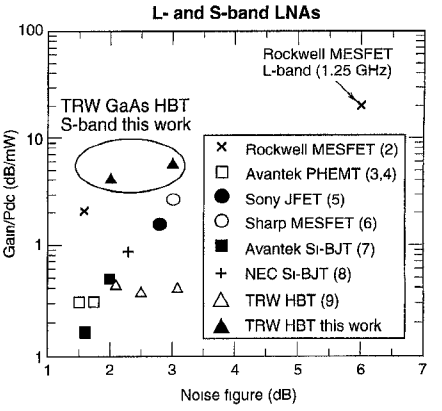


Fig. 1. Gain to dc power ratio plotted versus noise figure for several state-of-the-art L- and S-band LNA's.

I. Introduction

IN PORTABLE CONSUMER applications where conserving battery life directly impacts cost, obtaining high gain and low noise figure under low dc bias operation is highly desirable. GaAs HBT's are attractive for these applications because of their high device transconductance and linearity under low dc bias operation, small size, and low device noise figure capability at L-, S-, and C-band frequencies. Moreover, these applications which span frequencies up to 6 GHz and encompass the new ISM bands, can be supported by a low cost GaAs HBT fabrication process which utilizes relaxed 2 and 3 μm emitter width geometries.

A demonstration of an ultra-low dc power GaAs HBT amplifier which achieved 13.1 dB gain with only 5 mW of dc power, and a record gain to dc power ratio (Gain/P_{dc}) of 2.6 dB/mW at X-band was previously reported [1]. However, no previous results on the noise and gain performance of an ultra-low dc power HBT L-, S-, or C-band amplifier have been reported until this work. Fig. 1 shows a graph of Gain:P_{dc} ratio plotted versus noise figure for several state-of-the-art L- and S-band LNA's [2]–[9]. A Gain/P_{dc} ratio of 19.1 was demonstrated with MESFET technology and is the highest reported to date. However, this is at a frequency of 1.25 GHz (L-band) and the corresponding noise figure is 6 dB [2]. The HBT LNA of this work obtained Gain/P_{dc} ratios of 4.2 and 5.65 at 2.0 GHz which are the highest reported at S-band, and achieved noise figures of 2.0 dB and 3.01 dB, respectively.

Low chip cost is also important in high volume consumer applications. GaAs MMIC's can offer higher performance than silicon IC's at these frequencies, but usually at the expense of higher cost. Thus, realizing compact chips with high performance is very important in GaAs commercial production technology. Usually there is a performance-size (cost) trade-off that can be illustrated by plotting chip size versus Gain/NF · P_{dc} ratio, which is a figure of merit measuring the utility of an LNA for low power portable applications [6]. Fig. 2 shows a plot of chip size versus Gain/NF · P_{dc} ratio for various L- and S-band LNA's. This figure illustrates that higher performance is achieved at the expense of larger chip size. Fig. 2 also shows that a MESFET LNA achieves a Gain/NF · P_{dc} ratio of 3.0 (1/mW) which is the highest reported at L-band. The GaAs HBT LNA of this work achieves a Gain/NF · P_{dc} ratio of 2.1 (1/mW) which is the highest reported at S-band, and is 4–5 times smaller in area than the L-band MESFET LNA. The HBT LNA is <1 mm^2 and is comparable in size to several of the other L-band LNA chips which have much poorer Gain/ · P_{dc} ratio figures of merit. An attractive feature of the HBT is that at reasonably low dc bias currents the gamma opt impedance (minimum noise source impedance) is close to a real 50 Ω impedance, with little reactive (inductive) component. This allows the use of physically smaller spiral inductors to match for minimum noise which results in a saving in chip area. Thus, the gamma opt

Manuscript received February 20, 1995; revised July 10, 1995.
The authors are with TRW Electronics Systems and Technology Division, Redondo Beach, CA 90278 USA.
IEEE Log Number 9415445.

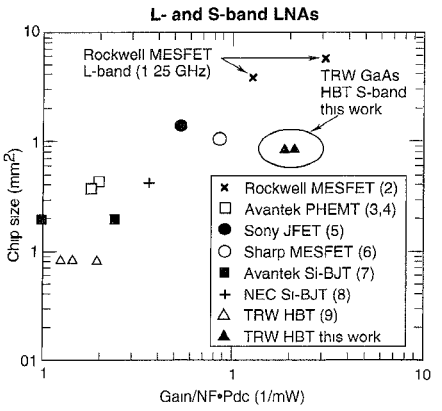


Fig. 2. Chip size versus Gain/NF·P_{dc} ratio for the various L- and S-band LNA's.

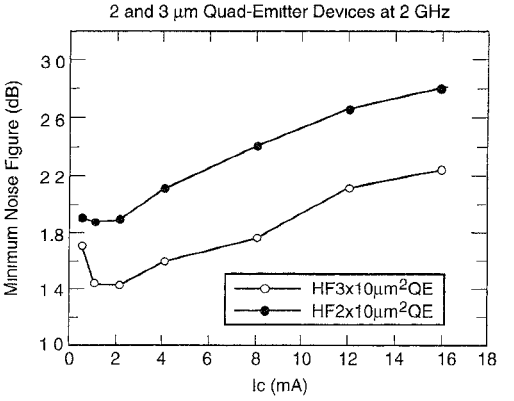


Fig. 3. Minimum noise figure of both 2- and 3-μm HBT quad-emitter devices as a function of collector current at 2 GHz.

characteristics of HBT's can accommodate low noise figure performance in a reasonably compact area.

In addition, a C-band self-biased HBT LNA design targeted for the high ISM band applications demonstrated a record noise figures of 2.4 dB at 5 GHz and was self-biased through a 3.5 V supply. This extends the state-of-the-art LNA noise figure performance by 0.5 dB over previous HBT LNA work. Furthermore, simulations suggest that the minimum achievable amplifier noise figure could be improved by as much as 0.5 dB by using spiral inductors with lower conductor loss.

The following sections will describe the low noise characteristics of the HBT device, and the design and measured performance of the S- and C-band HBT LNA's.

II. GaAs HBT Low Noise Process Technology

The LNA's were fabricated with TRW's AlGaAs/GaAs HBT foundry technology. The MBE profile of our standard GaAs HBT process incorporates a base thickness of 1400 Å uniformly doped to 1×10^{19} cm^{-3}, a collector thickness of 7000 Å lightly doped N-type of 7×10^{15} cm^{-3}, and an N^+ sub-collector doped to 5×10^{18} cm^{-3}. The HBT process incorporates a self-aligned base ohmic metal (SABM) technique for fabricating both 2- and 3-μm emitter width HBT's. The resulting HBT transistors have an f_T and f_{max} of 23 GHz and 50 GHz, respectively.

Device noise parameters were measured on-wafer for both 2 $\times$ 10 μm^2 quad-emitter (total emitter area = 4$\times$ 2 $\times$ 10 μm^2) and 3 $\times$ 10 μm^2 quad-emitter (total emitter area = 4 $\times$ 3 $\times$ 10 μm^2) HBT devices using an ATN automatic noise parameter test set. Fig. 3 gives the minimum noise figure of both the 2- and 3-μm HBT devices as a function of collector current at 2 GHz. Over bias current, a 0.5 dB improvement in device minimum noise figure is seen for the 3-μm HBT over the 2-μm HBT device. The noise improvement of the 3-μm HBT may be explained by the lower emitter contact resistance which results in lower thermal noise. Due to the larger emitter stripe area of the 3 $\times$ 10 μm^2 quad-emitter HBT, the emitter resistance is $\approx$1.5 Ω which is 40% smaller than the emitter resistance of the 2 $\times$ 10 μm^2 quad-emitter HBT which is 2.5 Ω. The dc betas of both the 2 and 3 μm HBT's are typically 30–40 at a collector current of 2 mA (the two devices are operating at different current densities). The drawback of the 3-μm HBT is that it will have poorer amplifier frequency capability due to the larger junction capacitances and higher base resistance. However, for frequencies <6 GHz, this does not become a significant factor in the circuit performance. Fig. 3 also illustrates that as the collector bias current is decreased, the minimum noise figure of both HBT devices decreases until a collector current of about 2 mA is reached. From 2 mA down to 0.5 mA the minimum noise figure of the devices levels off. This bias dependent characteristic was also observed at 1, 3 and 6 GHz. For HBT devices, lower current generally means lower minimum noise. However, for low noise amplifier design, the source impedance required to achieve minimum noise (gamma opt) needs to be considered over bias. This point is especially important for amplifiers which extend into the microwave frequency range.

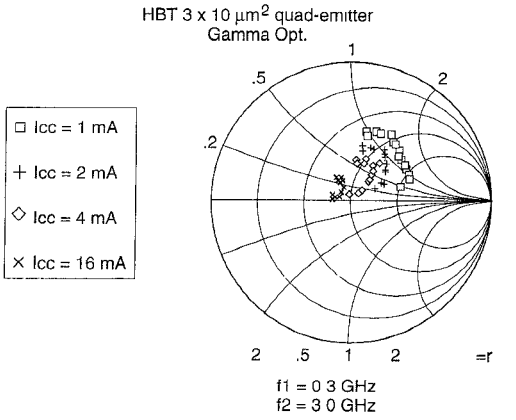


Fig. 4. Optimum noise source impedance (gamma opt.) loci plotted from 300 MHz to 3 GHz of a 3 $\times$ 10 μm^2 quad-emitter HBT device for several different collector currents.

Fig. 4 shows a plot of the optimum noise source impedance (gamma opt.) from 300 MHz to 3 GHz of a 3 $\times$ 10μm^2 quad-emitter HBT as a function of collector current. The impedance plot shows that at lower currents the optimum impedance has a large real part, greater than 50 ohms, with a significant inductive reactance. For higher collector currents, gamma opt. is mostly real and decreases below 50 ohms. At 16 mA, the impedance is close to 50 ohms over the frequency range. At

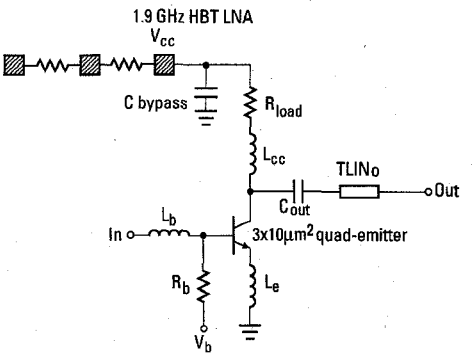


Fig. 5. Schematic of the 2 GHz low dc power, low noise HBT amplifier.

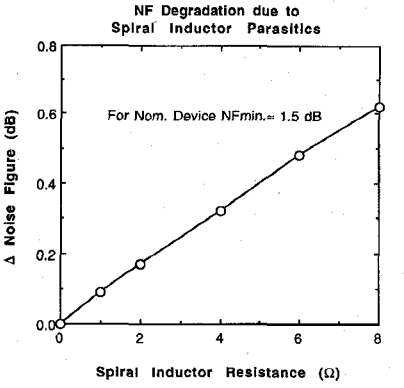


Fig. 6. Degradation in LNA NF as a function of the series parasitic resistance of the base-tuned spiral inductor, L_b.

this bias point, the gamma opt. is nearly coincident with 50 ohms which makes it easier to design both good input return-loss and low noise figure over a broad band, however the minimum achievable noise figure at this bias will be higher than at lower bias currents. For low noise and low dc bias operation, a design employing series inductive matching at the input of the HBT device will result in optimum noise match over a narrow band. The design of a 2.0 GHz S-band and a 5.7 GHz C-band low noise amplifier using this series base inductor matching topology is described below.

III. S- AND C-BAND HBT LOW NOISE AMPLIFIERS

A schematic of the 2 GHz low dc power, low noise HBT amplifier is shown in Fig. 5. The amplifier is a one-stage narrow-band design which is matched for a center frequency of 1.9–2.0 GHz. A 3.8 nH input series inductor, L_b, is used to match the input of a 3 × 10 μm^2 quad-emitter HBT for minimum noise. A collector bias current of 1 mA and a V_{ce} = 2.0 V was chosen in order to realize a gain greater than 8 dB and a minimum noise figure less than 2.0 dB with a total power consumption of 2 mW at 2 GHz. A 0.5 nH spiral inductor, L_e, in series with the emitter of the HBT device is used to tune gamma opt so that it coincides more closely to the 50 Ω source impedance in order to achieve optimum noise and input return-loss match. This is a conventional low noise microwave matching technique which is common among MESFET and HEMT LNA designs. The output of the amplifier is matched using a series L-C matching network comprised of C_{out} and TLIN$_o$. An inductive choke L_c, in series with a small load resistance, R_{load}, provides both a high-pass ac load and a means for biasing the collector of the HBT device.

The amplifier was designed for minimum noise figure at 1.9 GHz. The LIBRA simulated noise figure using device noise and s-parameters was 1.7 dB while the measured minimum noise figure was 1.9 dB. This 0.2 dB discrepancy is well within measurement error and process variations. The minimum measured noise figure of a 3 × 10 μm^2 quad-emitter HBT at this frequency is ≈1.3 dB at low dc bias. Approximately 0.4 dB noise figure is attributed to the series resistive losses of the nonideal spiral inductors L_b and L_e, which have values of 3.8 nH and 0.5 nH, respectively. These lossy spiral inductors have 5 Ω and 0.5 Ω of effective series resistance, respectively, which is attributed to conductor losses of the two interconnect metals constructing the spiral inductors. Plated Au top metal which is ≈3.5μm thick is used to construct the spiral inductor windings while ≈800 Å of evaporated Au is used to construct the spiral inductor center feed. Fig. 6 illustrates the impact that the series parasitic resistance of the base-tuned spiral inductor, L_b, has on the noise figure of the HBT LNA. This chart applies for HBT LNA's which use HBT's with minimum device noise figures of ≈1.3–1.5 dB. This figure shows that the amplifier noise figure increases linearly with the spiral inductor parasitic series resistance. dc measurements of the spiral inductors indicate that the parasitic series resistance is dominated by conductor losses of the interconnect metals rather than skin effect at these low frequencies. Thus, for low frequency L-, S- and C-band LNA's, spiral inductors with thicker metal and/or wider line widths would help reduce the spiral inductor series resistance and result in improved amplifier noise figure performance.

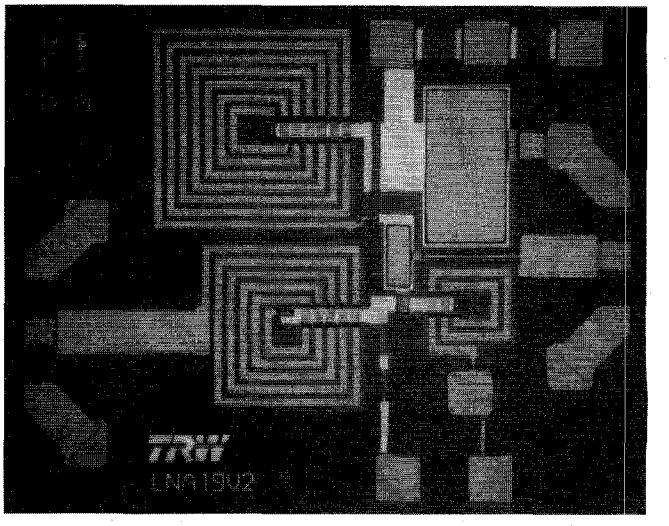


Fig. 7. Microphotograph of the 1.9 GHz single stage low noise amplifier chip. The total chip area is 1.05 × 0.82 mm^2.

Fig. 7 shows a microphotograph of the 2.0 GHz single stage low noise amplifier chip which is 1.05 × 0.82 mm^2 in area. Square inductors were used to minimize the required area of the passive components. Much of the wasted area is consumed by 50 Ω transmission lines and the on-wafer rf probe pad configuration. A production layout of this chip can be reduced by 40%, including a self-biasing network.

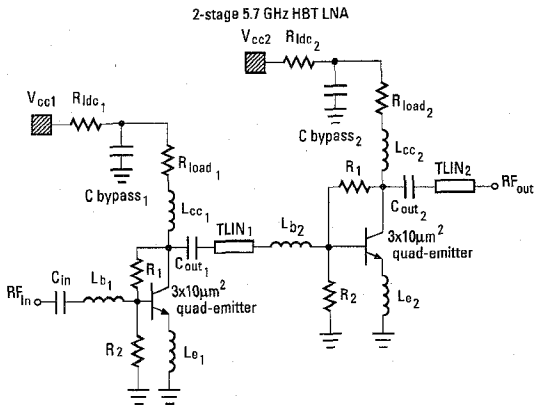


Fig. 8. Schematic of the 2-stage C-band self-biased HBT LNA.

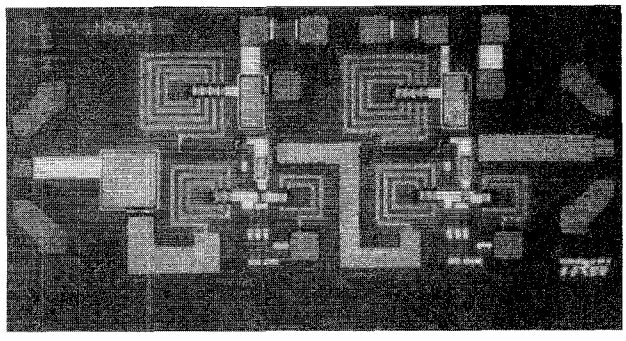


Fig. 9. Fabricated 2-stage C-band LNA chip. Chip size is 1.59 × 0.83 mm^2.

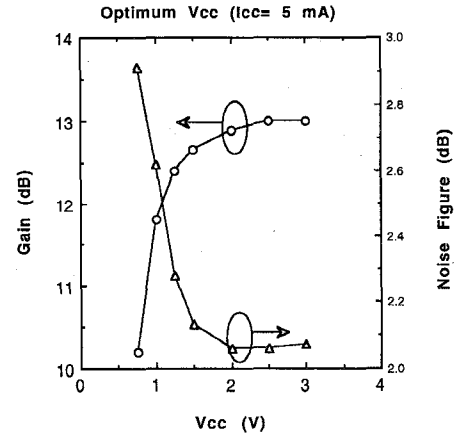


Fig. 10. Gain and noise figure performance at 2 GHz as a function of bias voltage $V_{cc}(I_{cc} = 5$ mA).

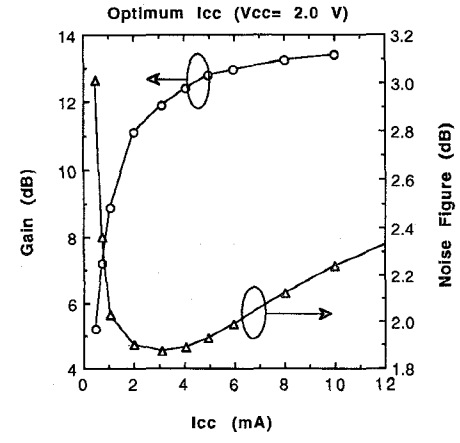


Fig. 11. Gain and noise figure performance at 2 GHz as a function of collector bias current $I_{cc}(V_{cc} = 2.0$ V).

A 5.7 GHz C-band HBT LNA was also designed using the same narrow-band noise matched topology. A schematic of the 2-stage C-band LNA is shown in Fig. 8. At this C-band frequency 2-stages are used in order to obtain reasonable gain. In addition, resistive self-biasing comprised of resistors R_1, R_2 and R_{Ldc}, is used to simplify the biasing of the circuit which is convenient for on-wafer evaluation. The dc current through the resistive bias network is on the order of 0.2 mA per stage to ensure proper operation over variations in dc beta from wafer to wafer. Each stage of the amplifier employs 3 × 10 μm^2 quad-emitter devices which are nominally biased at an I_{ce} = 8–10 mA and V_{ce} = 2 V. At this bias, a nominal gain >15 dB and noise figure of 2.9 dB are predicted at 5.7 GHz. The device minimum noise figure at this frequency is 2.52 dB. Approximately 0.4 dB of this noise figure is attributed to the losses of the spiral inductors in series with the base of the HBT's. Fig. 9 shows the fabricated 2-stage C-band LNA chip. The chip size is 1.59 × 0.83 mm^2 and is only 1.5 times larger than the single-stage S-band LNA. Two dc pads at the top of the chip are used to self-bias the LNA through a fixed 3.5 V voltage supply.

IV. Measurements and Discussion

Noise figure and gain were measured for the S-band LNA at different bias conditions in order to find the optimum noise bias of the amplifier. Fig. 10 shows gain and noise figure performance at 2 GHz as a function of voltage (V_{cc}) for a fixed collector current, I_{cc} = 5 mA. This figure shows that at a $V_{cc} \geq 2.0$ V, the amplifier achieves minimum noise figure and maximum gain performance. This may be explained by the fact that the collector-base capacitance is fully depleted under reverse biases of greater than about 0.6 V which corresponds to a $V_{cc} \approx V_{ce} = 2.0$ V. This characteristic is dependent on the material structure of the collector and base of the HBT. At this optimum collector voltage, the gain and noise figure were measured as a function of collector bias current (I_{cc}) at 2 GHz, and are given in Fig. 11. This figure shows that the optimum low noise bias current (I_{cc}) is between 2 mA and 4 mA for the HBT LNA. At currents slightly lower than 2 mA the noise figure begins to ramp up very quickly due to a rapid change in the gamma opt over bias. A figure of merit which measures the utility of an LNA under low dc power consumption is the Gain/NF · P_{dc} ratio (1/mW) and has been previously defined [6]. At an optimum collector bias of 1.04 mA and 2.1 mW power consumption, the corresponding Gain/NF · P_{dc} ratio figure of merit is 2.10 (1/mW) which is the highest reported at S-band for any technology.

Fig. 12 shows the measured gain, noise figure, and return-loss of the amplifier at optimum low noise bias (I_{cc} = 2 mA and a V_{cc} = 2.0 V). The nominal gain is 11.1 dB at 2.0 GHz with a corresponding input and output return-loss of −13.7 dB and −14.7 dB, respectively. The amplifier has a

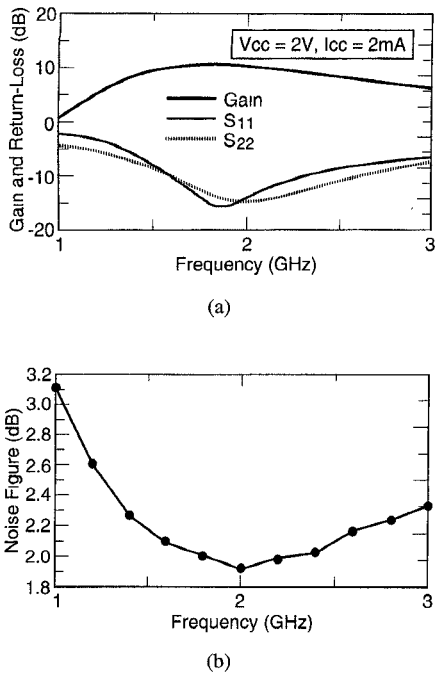


Fig. 12. Measured (a) gain and return-loss, and (b) noise figure performance at an I_{cc} = 2 mA and a V_{cc} = 2.0 V.

40% 1-dB bandwidth from 1.5–2.3 GHz. Fig. 12 also shows the broadband noise figure performance. Over a 1.5–2.8 GHz bandwidth, the noise figure ranges from a minimum of 1.9 dB to a maximum of 2.2 dB. Under a very low dc collector current bias of 0.46 mA and a total power consumption of 0.92 mW through 2 Volts, the gain and noise figure are 5.2 dB and 3.1 dB, respectively, at 2 GHz. At this low dc bias, the gain:P_{dc} ratio is 5.65 dB/mW which is also the highest reported for an S-band amplifier.

Fig. 13 gives the P_{1-dB} output compression and IP3 performance at 2 GHz as a function of collector bias current (I_{cc}). At a low noise bias of 2 mA and V_{cc} = 2.0 Volts, the corresponding IP3 and P_{1-dB} are 11 dBm and 0 dBm, respectively. At an ultra-low dc bias of 0.46 mA and V_{cc} = 2.0 Volts, the corresponding IP3 is −2.8 dBm. The P_{1-dB} compression was measured for both a V_{cc} = 2.0 and 3.0 Volts as a function of bias current (I_{cc}). At a V_{cc} = 3 Volts, the 1-dB compression was found to be 3–4 dB higher at the higher current bias. Fig. 13 also illustrates that for higher bias currents >2 mA and a fixed V_{cc} = 2.0 V, the delta between the IP3 and P_{1-dB} is 15 dB. This is greater than the "10 dB delta rule of thumb" assumed for conventional FET amplifiers. This suggests that higher amplifier linearity can be achieved from HBT's than from FET's for a given output power (P_{1-dB}). This means that greater spurious free dynamic range can be obtained from HBT's which is attractive for frequency dense receiver applications such as spread spectrum wireless systems.

The noise figure, gain, and IP3 performance of the 5.7 GHz C-band LNA were also characterized as a function of bias condition. Fig. 14 shows the gain and noise figure at 5.7 GHz as a function of total collector bias current, I_{cc}, of both stages. The minimum noise figure at 5.7 GHz is 2.9 dB at a collector

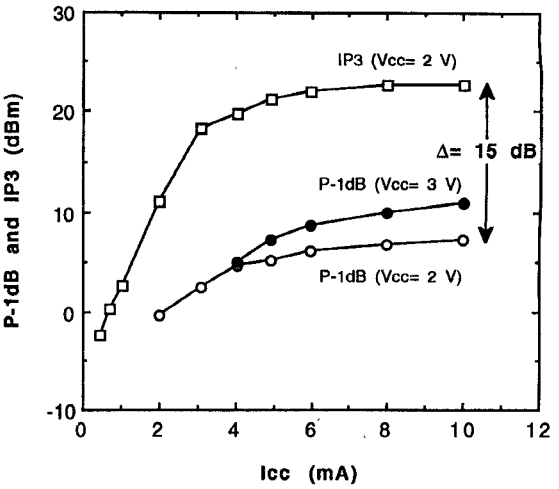


Fig. 13. P_{-1dB} output compression and IP3 performance at 2 GHz versus collector bias current, I_{cc}.

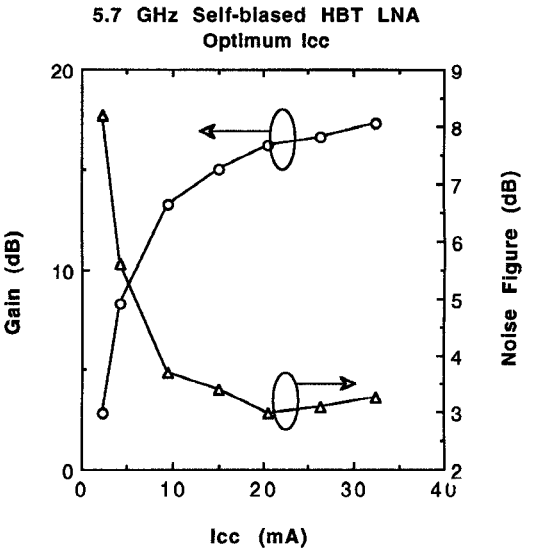
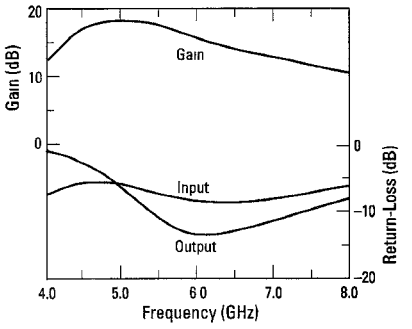
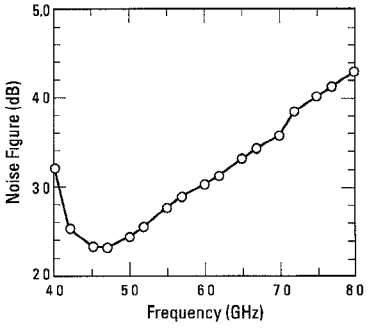


Fig. 14. Measured gain and noise figure at 5.7 GHz as a function of total collector bias current, I_{cc}.

bias of 20.6 mA. The corresponding gain is 16.2 dB. This bias corresponds to an I_{ce} ≈10 mA per 3 × 10μm^2 quad-emitter device. The supply voltage is 3.5 V and the total power consumption is 72 mW. Fig. 15 shows a broadband response of the amplifier at this bias current which indicates a peak gain of 18.2 dB at 5 GHz. The input return-loss is 7 dB while the output return-loss is >12 dB. Both input and output return-losses are centered about 5.7 GHz. The minimum noise figure is 2.4 dB and occurs at the maximum gain frequency of 5 GHz. This noise figure is 0.5 dB lower than a previously reported HBT LNA which achieved 3.1 dB at 4.5 GHz [9]. This is illustrated in Fig. 16 which summarizes previously reported MMIC LNA noise figure performance for frequencies below 10 GHz. This plot shows that the S- and C-band HBT LNA MMIC's of this work achieve low noise figures which are comparable to previously reported MMIC LNA's based on various FET and bipolar technologies. The minimum device



(a)



(b)

Fig. 15. Measured broadband (a) gain and return-loss, and (b) noise figure performance at an $I_{cc} = 20.6$ mA and a $V_{cc} = 3.5$ V.

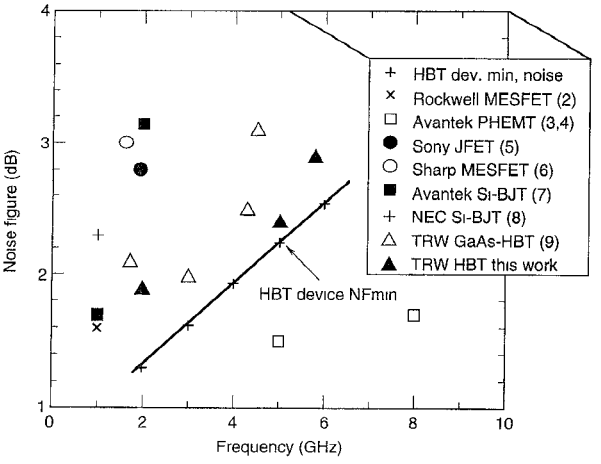


Fig. 16. State-of-the-art LNA noise figure performance for frequencies below 10 GHz.

noise figure of a typical HBT biased at low dc current is also plotted. Relative to this device NF_{min}. curve, the S- and C-band HBT LNA's of this work achieve noise figures which are within 0.5 dB of the device minimum achievable noise figure. The 0.5 dB increase in LNA noise figure over the HBT device NFmin. is attributed to spiral inductor conductor losses as explained in the previous section.

Finally, the IP3 and P_{-1dB} output characteristics of the C-band LNA were measured over bias, given in Fig. 17. This plot shows that an IP3 and P_{-1dB} are as high as 23.5 dBm and 9.5 dBm, respectively, under high bias operation. A unique characteristic of these HBT LNA's, which was already

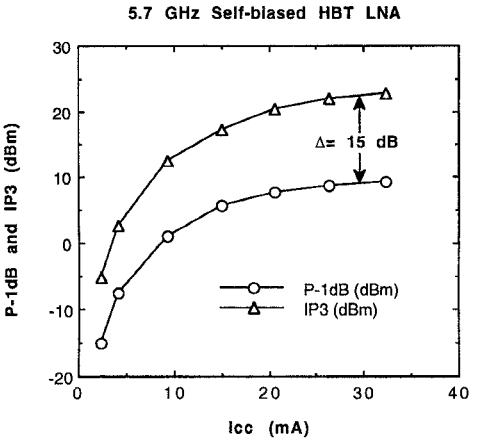


Fig. 17. IP3 and P_{-1dB} output characteristics of the C-band LNA as a function of bias current, I_{cc}.

pointed out for the S-band LNA, is that the IP3 is ≈15 dB greater than the P_{-1dB}. This claim is also supported by the measured output characteristics of the C-band LNA given in Fig. 17. This high linearity characteristic is another feature which makes these HBT LNA's attractive for low dc power wireless receiver applications.

V. Conclusion

A 2.1 mW ultra-low dc power GaAs HBT LNA with 2.0 dB noise figure and 8.9 dB gain was achieved at 2 GHz. The corresponding Gain/NF · P_{dc} ratio figure of merit is 2.10 (1/mW) which is the highest reported at S-band. Under low dc power bias of 2 V and 0.46 mA, or 0.92 mW of power consumption, the amplifier achieves 5.2 dB gain, 3.01 dB noise figure and a Gain/P_{dc} figure of merit of 5.65 (dB/mW) which benchmarks the highest reported gain to dc power ratio (Gain/P_{dc}) in this frequency band. In addition, a C-band self-biased HBT LNA achieved a record 2.4 dB noise figure at 5 GHz. This amplifier achieves 0.5 dB improvement in NF over previously reported HBT LNA's. Both HBT LNA's were shown to be limited in noise performance by the parasitic resistances of the spiral inductors comprising the gamma opt. input matching network. In each case, the LNA NF's were as much as 0.5 dB higher than the minimum HBT device NF. High linearity was also demonstrated by both HBT LNA's, which obtained IP3's which were 15 dB greater than their respective P_{-1dB}, suggesting superior linearity performance to conventional FET's. The high performance obtained from these HBT LNA's under very low dc bias, and the low cost nature of GaAs HBT fabrication technology, make them attractive for portable wireless consumer applications.

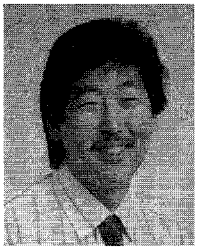
Acknowledgment

The authors would like to thank G. Fisk for his technical support in low noise device and circuit characterization.

References

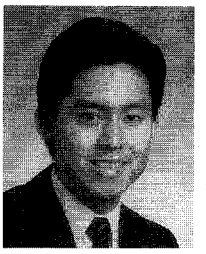
[1] K. W. Kobayashi, A. K. Oki, L. T. Tran, D. K. Umemoto, and D. C. Streit, "5 mW GaAs HBT low power consumption X-band amplifier," in

1994 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig., San Diego, CA, pp. 147–150.
[2] K. R. Cioffi, "Monolithic L-band amplifiers operating at milliwatt and sub-milliwatt dc power consumptions," in *1992 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig.*, Albuquerque, NM, pp. 9–12.
[3] H. Morkner, M. Frank, and R. Kishimura, "A novel MMIC PHEMT low noise amplifier for GPS applications," in *1992 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig.*, Albuquerque, NM, pp. 13–16.
[4] H. Morkner, M. Frank, and D. Millicker, "A high performance 1.5 dB low noise GaAs PHEMT MMIC amplifier for low cost 1.5–8 GHz commercial applications," in *1993 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig.*, Atlanta, GA, pp. 13–16.
[5] T. Ohgihara, S. Kusunoki, M. Wada, and Y. Murakami, "GaAs JFET front-end MMIC's for L-band personal communications," in *1993 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig.*, Atlanta, GA, pp. 9–12.
[6] S. Hara, K. Osato, A. Yamada, T. Tsukao, and T. Yoshimasu, "Miniature low noise variable MMIC amplifiers with low power consumption for L-band portable communication applications," in *1993 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig.*, Atlanta, GA, pp. 67–70.
[7] I. Kipnis, J. F. Kukielka, J. Wholey and C. P. Snapp, "Silicon bipolar fixed and variable gain amplifier MMIC's for microwave and lightwave applications up to 6 GHz," in *1989 IEEE Microwave Millimeter-Wave Monolithic Circuit Symp. Dig.*, Long Beach, CA, pp. 101–104.
[8] H. Takeuchi, M. Muraoka, T. Hatakeyama, A. Matsuoka, M. Honjou, S. Miyazaki, K. Tanaka, and T. Nakata, "A Si wide-band MMIC amplifier family for L-S band consumer product applications," in *1991 IEEE Microwave Theory and Tech. Symp. Dig.*, Boston, MA, pp. 1283–1284.
[9] K. W. Kobayashi and A. K. Oki, "Sub-2.5 dB noise figure GaAs HBT direct-coupled LNA's for high volume commercial applications to 6 GHz," in *1994 IEEE GaAs IC Symp. Dig.*, Philadelphia, PA, pp. 303–306.



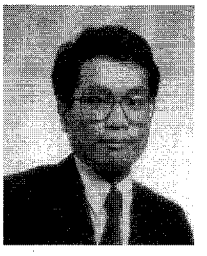
Kevin W. Kobayashi (M'93) was born in San Diego, CA in 1963. He received the B.S.E.E. from the University of California at San Diego in 1986, and the M.S.E.E. degree from the University of Southern California in 1991.

From 1985 to 1986 he worked for Burrough Micro-components Group in Rancho Bernardo, CA, where he worked on SPICE and 2–dimensional devices simulation and modeling of LDD MOSFET's. Since 1986 he has been working at TRW's Advanced Microelectronics Laboratory in Redondo Beach, CA, where he has been involved in the development of HBT, HEMT, and MESFET technologies. His primary focus is in the design of HBT and HEMT MMICS for insertion into TRW systems. He also provides technical design support and instruction for GaAs HBT commercial foundry customers. His research activities have included the development of HBT low phase noise VCO's for synthesizers, the development of broadband techniques for HBT amplifiers, active matching and feedback design development, design topology studies for high linearity VGA's, and the design of low noise receivers and LNA's employing TRW's HBT commercial foundry process for wireless applications. He has also been heavily involved with the development of Selective MBE MMIC's (under Dr. D. Streit and A. Oki) which integrate HEMT's, HBT's, PIN's, and high performance Schottky diodes on the same III–V substrate for next generation high performance mixed-mode MMIC applications. He has authored several technical papers on MMIC design and IC technology and has received several patents.



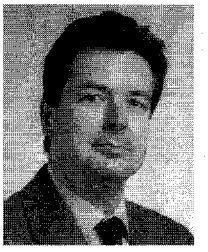
Aaron K. Oki (M'85) was born in Honolulu, Hawaii. He received the B.S. degree in electrical engineering in 1983 from the University of Hawaii, Manoa and the M.S. degree in electrical engineering and computer science in 1985 from the University of California, Berkeley.

Since joining TRW as a member of technical staff in 1985 he has been working on production and advanced development of HBT technology. In 1990 he became the principal investigator for HBT IR&D and section head of the HBT products section.



Liem T. Tran (M'86) received the B.S. degree in applied physics from the California Institute of Technology and the M.S. degree in electrical engineering from the University of California at Berkeley.

He has been at TRW since 1988 working on GaAs and InP-based HBT's.



Dwight C. Streit (S'81-M'86-SM'92) received the Ph.D. degree in electrical engineering from the University of California, Los Angeles in 1986.

He is currently manager of the Advanced Materials Section and assistant manager of the Microelectronics Product and Technology Development Department in TRW's RF Products Center. He is a TRW Technical Fellow and principal investigator for two research and development projects related to III–V materials and monolithic HEMT-HBT integrated circuit.